Iker Garcia Morales

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Electrical Engineering student with hands-on experience in digital design, VLSI layout, and hardware verification.
Skilled in Verilog/VHDL, CMOS layout (Electric VLSI), and simulation tools (ModelSim, Quartus).
Interested in CPU architecture, ASIC design, and next-generation semiconductor systems.

SKILLS:

Hardware Description Languages: Verilog, VHDL
Programming: C, C++, Python, MATLAB
VLSI & Digital Design: CMOS Layout (Electric), Digital Logic Design, ASIC Design Flow
Simulation & Tools: ModelSim, Quartus Prime, LTSpice
Embedded Systems: Arduino, ESP32
Other: Linux, Git, Simulink

EDUCATION:

John Brown University, Siloam Springs, AR
Bachelor of Science in Electrical Engineering, Double Major in Robotics and Mechatronics Engineering.
Expected Graduation: May 2027.
Relevant Coursework
Integrated Circuit Design: Electric VLSI, Embedded Systems, Electromagnetics, Electronics, Electrical Circuits, Digital Electronics, Control Systems.

PROJECTS:

VLSI Design Project: 8-bit MIPS Processor (Electric VLSI)
Designed and implemented an 8-bit MIPS CPU using a bitslice architecture, including datapath, control unit, and ALU.
Performed full-custom CMOS layout, passing DRC/ERC/NCC verification.
Simulated functionality using IRSIM and validated correct operation across multiple test scenarios.
Integrated core into padframe for chip-level design targeting MOSIS TinyChip process.
Implemented control logic using FSM-based controller and integrated datapath modules across 8-bit slices.

ASIC Design: Similarity Detector (Electric VLSI)
Designed and implemented an 8-bit similarity detector that outputs a match when the number of equal bits between two vectors exceeds a programmable threshold.
Developed modular logic blocks including an XNOR array, match counter, and comparator, and verified functionality through simulation.
Created schematic and CMOS layout in Electric VLSI and completed DRC, ERC, and NCC verification.

Digital Electronics:
Designed and simulated a serial 4-bit ALU at gate level using Quartus, implementing arithmetic and logic operations (add, subtract, XOR, increment). Developed sequential architecture using shift registers and carry logic,
and verified functionality through simulation and timing analysis.

RELEVANT WORK EXPERIENCE:

John Brown University — Siloam Springs, AR
Teaching Assistant – Digital Electronics
Jan 2025 – Present
Facilitated lab sessions on digital circuit design and troubleshooting, supported students in logic gates, flip-flops, multiplexers, and counters, graded assignments emphasizing circuit correctness and technical precision
Learning Coach – Student Support Services
Aug 2025 – December 2025
Provided structured academic support through one-on-one and small group sessions, strengthened student problem-solving skills and study strategies in technical coursework
General Tutor (Engineering & Math)
Sept 2024 – Present
Tutored Calculus and Electrical Circuits, reinforced circuit analysis techniques and mathematical foundations for engineering students

LEADERSHIP EXPERIENCE:

IEEE Club – Junior Senator
Student Government Association – Freshman Senator, Junior Senator.
Walton International Scholarship Scholar.